

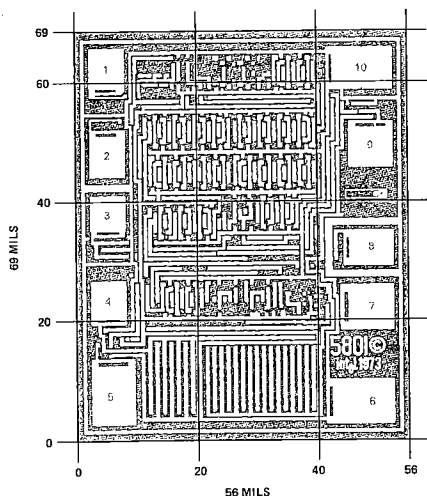
LOW POWER OSCILLATOR-DIVIDER

- Advanced Silicon Gate Ion Implanted CMOS Technology
- Long Battery Life--Low Current Drain--5 μ A max.
- On Chip Drive and Regulator Circuitry for Up-Converter
- Inputs Protected Against Static Discharge

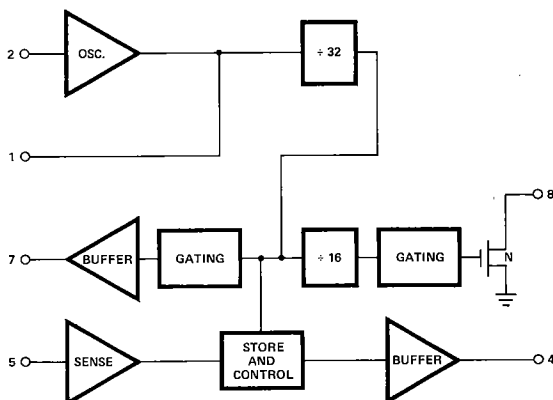
The 5801 is a low power oscillator and 2^9 divider ideally suited for use in battery powered timekeeping applications. The circuitry consists of an inverter stage designed to operate in conjunction with an external quartz crystal and feedback network to form an oscillator, a 9-stage binary ripple carry counter, and control logic. Two outputs are provided: A buffered drive output providing $\frac{1}{2}$ cycle of the oscillator at a repetition rate equal to the frequency of the oscillator divided by 2^5 and an open drain output that is switched on for $\frac{1}{2}$ cycle of the oscillator at a repetition rate of the oscillator divided by 2^9 . The buffered drive output and associated control circuitry are designed for use with external components to implement a regulated voltage up-converter.

The 5801 is manufactured with complementary MOS silicon gate technology. Long term continuous operation from small batteries is made possible by use of this low power technology.

CHIP TOPOGRAPHY
(Numbers refer to package pin number.)



BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias	−20°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage (V _{DD})	−0.3V to +8.0V
Voltage on Output (pin 8) with respect to V _{SS}	−0.3V to +18.0V
Voltage on all other pins	−0.3V to V _{DD} +0.3V
Power Dissipation	80mW

***COMMENT:**
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics (T_A = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I _{DD}	Average Supply Current		3.0	5.0	μA	V _{DD} = 1.4V, Note 1
V _{DDS}	Oscillation Start Voltage	1.2			V	Note 1
I _{OLC}	64 Hz N-Channel Open Drain Output Current	50			μA	V _{DD} = 1.2V; V _{OLC} = 1.2V
I _{OHD}	1024 Hz Drive P-Channel Output Current	−500			μA	V _{DD} = 1.2V; V _{OHD} = 0.7V
I _{OLD}	1024 Hz Drive N-Channel Output Current	200			μA	V _{DD} = 1.2V; V _{OLD} = 0.5V
I _{OLS}	1024 Hz Sample N-Channel Output Current	10			μA	V _{DD} = 1.2V; V _{OLS} = 0.15V
V _{IL}	Sense Low Input Voltage			0.4	V	V _{DD} = 1.2V
V _{IH}	Sense High Input Voltage	0.9			V	V _{DD} = 1.2V
V _{BDC}	64 Hz N-Channel Breakdown Voltage	15.0			V	V _{DD} = 1.2V; I _{BDC} = 1.0μA

Note 1. Frequency of oscillation = 32,768 Hz when connected as shown in Figure 1.

Test Circuit

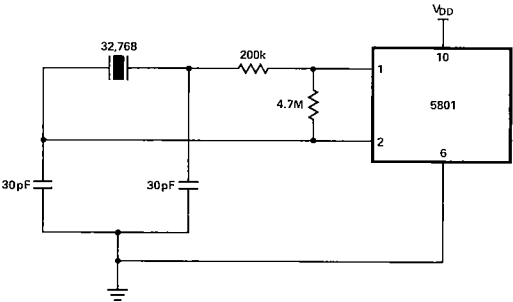


Figure 1.

A.C. Characteristics $T_A = 25^{\circ}\text{C}$

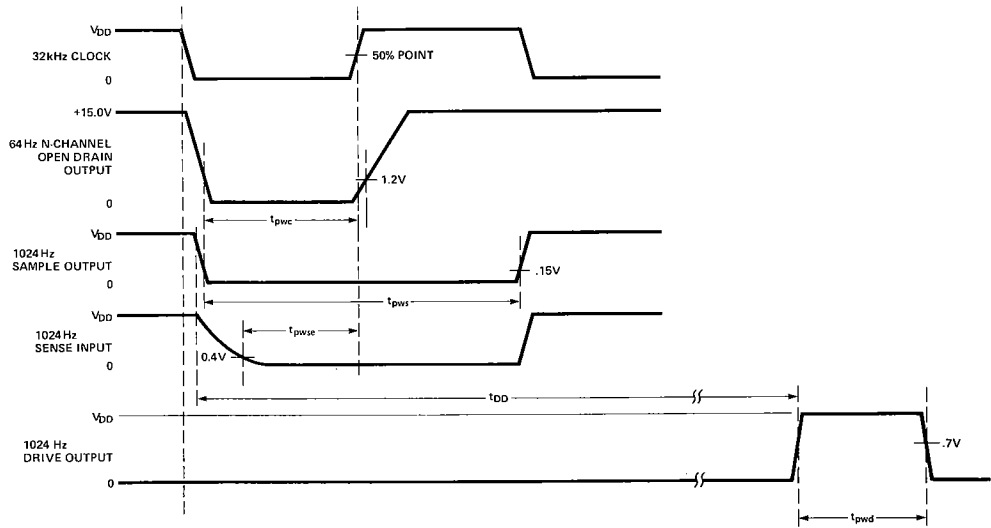
Symbol		Min.	Typ.	Max.	Unit	Test Conditions
t_{pwc}	64 Hz N-Channel Open Drain Output Pulse Width	10		25	μs	$V_{DD} = 1.2\text{V}, 1.4\text{V}; 64\text{Hz}$
t_{pws}	1024 Hz Sample Output Pulse Width	25		35	μs	$V_{DD} = 1.2\text{V}, 1.4\text{V}; 1024\text{Hz}$
t_{pwd}	1024 Hz Drive Output Pulse Width	13		17	μs	$V_{DD} = 1.2\text{V}, 1.4\text{V}; 1024\text{Hz}$
t_{dd}	1024 Hz Sample Output to Drive Output Delay	485		520	μs	$V_{DD} = 1.2\text{V}, 1.4\text{V}; 1024\text{Hz}$
t_{pwse}	1024 Hz Sense Input Pulse Width	5			μs	$V_{DD} = 1.2\text{V}, 1.4\text{V}; 1024\text{Hz}$

Capacitance

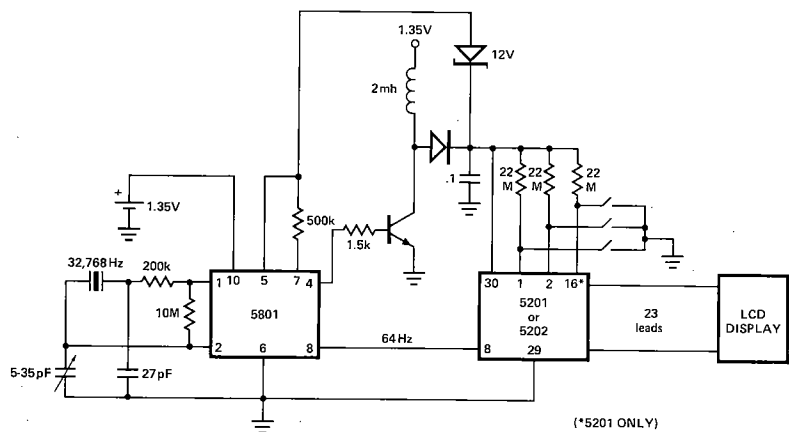
Symbol	Test	Typ.	Max.	Unit
C_{IN2}	Input Capacitance at pin 2 $V_{IN} = 0\text{V}$	3.2	8.0	pF
C_{IN5}	Input Capacitance at pin 5 $V_{IN} = 0\text{V}$	2.2	6.0	pF
C_{OUT1}	Output Capacitance at pin 1 $V_{OUT} = 0\text{V}$	3.0	8.0	pF
C_{OUT4}	Output Capacitance at pin 4 $V_{OUT} = 0\text{V}$	23	35	pF
$C_{OUT\ 7,8}$	Output Capacitance at pins 7,8; $V_{OUT} = 0\text{V}$	2.4	6.0	pF

Note: All capacitance values are measured in 10 lead flatpack with pins 6, 10 and all other untested pins tied to ground.

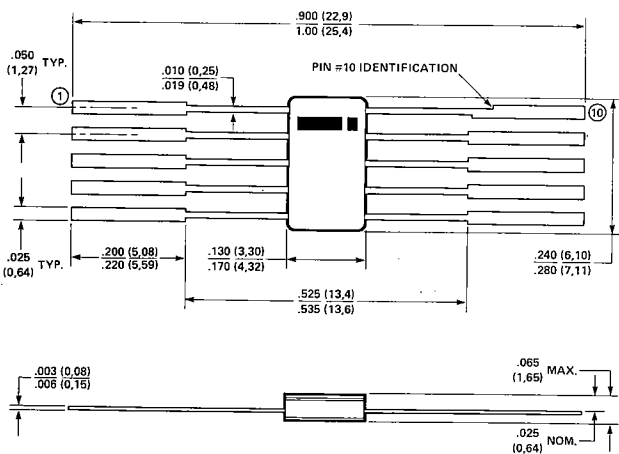
Timing Diagram



Typical Application



Packaging Information



PIN ASSIGNMENT

Pin #	Function
1	OSC INV OUT
2	OSC INV IN
3	N/C
4	1024Hz OUT (Drive)
5	1024Hz IN (Sense)
6	GROUND
7	1024Hz OUT (Sample)
8	64Hz OUT (N-CH)
9	N/C
10	V _{DD}